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DIY Gain-Blocks

The division of a high-frequency circuit into blocks which display a uniform system resistance Z_o at their inputs and outputs, has many advantages. The blocks can be connected to one another by cables of almost any length with the same system resistance without any change in the characteristics of the overall pattern. Individual blocks can be replaced by others with different characteristics to improve specific characteristics of the overall pattern, and all of them can be individually measured in an uncomplicated way, using measuring equipment with the system resistance.

1. INTRODUCTION

Gain-blocks are usually supplied for a system resistance of 50Ω and for the amplification of UHF frequencies. The advantages of block assembly can also be made use of in any other frequency range, and thus even for low frequency with Z_o = 600Ω, carrier frequency with Z_o = 150Ω and for TV/video with Z_o = 75Ω. The observations below also permit the dimensioning of gain-blocks for values of Z_o which deviate from 50Ω, a field which is not covered by commercially available MMIC's. It is even possible to match many characteristics to the application, within specific limits, such as lack of noise, freedom from distortion, lack of feedback and output.

2. COMMERCIALLY AVAILABLE GAIN-BLOCKS

Fig.1 shows some internal circuits. They can be relatively simple, or even complicated. One or more active elements are present, which are recipro-

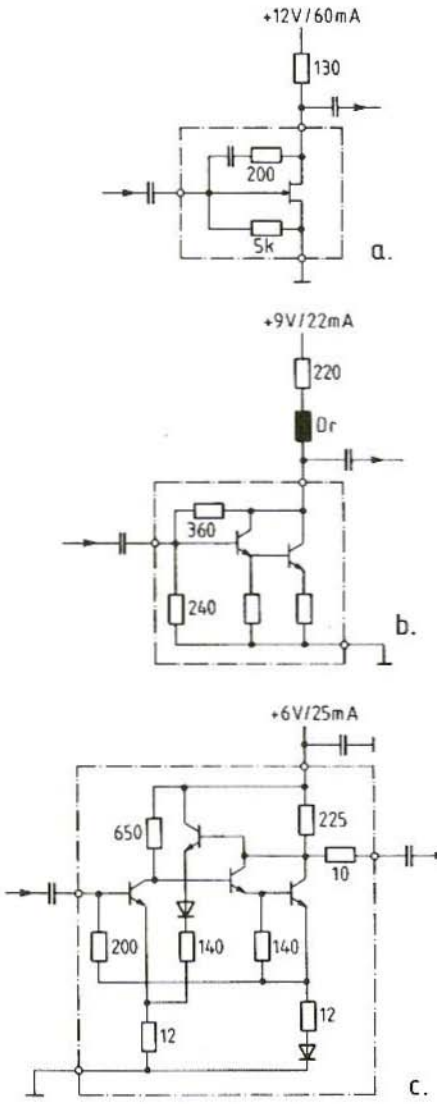

Fig.1: Some commercially available Gain-Blocks

a. Siemens CGY 40; V=2.8; 0.8-1.8 GHz - 1dB

b. Avantek MSA 07; V =4.7; 0.1-0.75 GHz - 1dB

c. Signetics 5205; V=8.9; 0.1-500 MHz - 1dB

cally linked in such a way that stable amplification occurs over a wide frequency range, with matching to Z_o at both gates. Resistance values shown in Fig.1 stem in part from the corresponding publications by the author (4...7) or were measured on specimens, as far as this can be done from outside. The diagram also shows the minimum circuit required: coupling and decoupling capacitors, sometimes resistances for power supply and setting the point of operation. For higher demands, chokes, Zener diodes, transistors and additional resistances also become necessary, in accordance with (4). Commercially available gain-blocks are thus in no way free from peripherals.

3. SEMI-CONDUCTORS FOR DIY GAIN-BLOCKS

An individual transistor with a reciprocally coupled resistance forms a gain-block in itself, which needs no more peripherals than a purchased unit. I shall try to restrict myself in what follows to layouts using only a single transistor, because otherwise the advantage over purchased equipment of having a single housing is lost and the calculations become very complicated.

Bipolars in an emitter circuit or FET's in a source circuit can be used as the transistors. Without reciprocal coupling, their amplification at low frequencies in a system using Z_o, without taking all higher-order terms into account, will be:

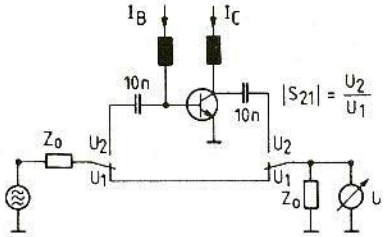

Fig.2: Circuit for measurement of S_{21}

$$V_{bip} = -\frac{2 \cdot \beta \cdot I_c \cdot Z_o}{Z_o \cdot I_c + \beta \cdot U_T} \quad (1a)$$

for bipolar transistors and

$$V_{fet} = -2 \cdot S \cdot Z_o \quad (1b)$$

for FET's.

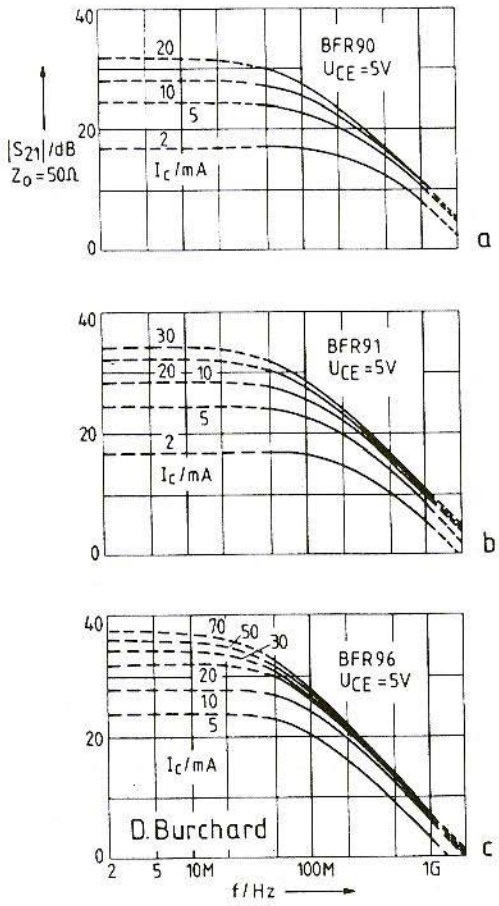

Fig.3: Scatter parameters S_{21} of some Bipolar Transistors

In the equations, U_T stands for the temperature voltage (0.028V) and S for the steepness. V is always negative, because the amplifiers invert. With a bipolar transistor any strong dependence on the collector current I_c disappears. The amplification calculated in this way is the maximum available and corresponds roughly to the scatter parameter, S_{21}. For many high-frequency transistors, you will find lists in the data sheets from which S_{21} can be read off. In all cases, you can measure the scatter parameter yourself in a measurement circuit - Fig.2. It stands to reason that a gain-block will always have less amplification than the maximum available. The reverse feedback to be attached will sap a good part of it, though this is repaid by an increase in the frequency range and an improvement in the balancing at the input and output.

At high frequencies, the maximum amplification available also decreases. For a bipolar transistor, we can distinguish several limiting frequencies:

f_s with regulated base voltage, and

f_β with regulated base current.

Both apply for any load resistor, however small (here Z_o). If the load resistance is high, then a third limiting

frequency must be taken into consideration, which is calculated from the load resistor and the output capacitance. It depends on the collector current of the transistor whether f_s or f_β determines the reduction in amplification. The transition from impressed base voltage to impressed base current takes place at $Z_o \cdot I_c = \beta \cdot U_T$. The input resistance R_{BE} of the transistor then has precisely the value of Z_o. For R_{BE}:

$$R_{BE} = \beta \cdot \frac{U_T}{I_c} \qquad (2)$$

Several limiting frequencies also become effective with an FET:

- f_s for decrease of 3dB in steepness
- f_e from source resistance and input capacitance (including Miller capacitance)
- f_a from load resistor and output capacitance.

It is much easier to look at the S_{21} curve than to calculate the limiting frequencies. For several popular high-frequency transistors and some FET's, these are as shown in Figs. 3 and 4. The dotted curves in Fig.3 are extrapolations corresponding to theoretical considerations. Solid sections of the curve correspond to the published S_{21} lists. The curve for CFY 19 in Fig.4 corresponds to the published values. The power FET curves were taken from a circuit like Fig.2. They serve a similar purpose here to those for the open-loop voltage gain of an operational amplifier. It can be seen at a glance how far the amplification should be reduced to obtain a specific frequency range, and how much reserve amplification the circuit has in a reciprocally linked condition. It can be seen immediately from Fig.3 that the BFR 90 is the best of the three transistors shown for all currents below 20mA. The BFR 91 is more favourable only in a narrow current range from 20 to 30mA, and the BFR 96 offers greater amplification only below 100 MHz at still higher current levels. Below 45°, there is a decrease as the frequency increases, which indicates, as with operational amplifiers, that reverse feedback of any strength is possible without instability.

The high-frequency reduction in amplification for the FET's in Fig.4 is variable. The curve at 10 GHz stops at CFY 19, so no more precise information can be obtained. This transistor is not suitable for gain-blocks, because it offers too little reserve amplification.

As we shall see later, only 12dB is lost through the matching requirement, so that useful amplification can be supplied in a 50Ω system.

The curves for U 244 and VN 10 KM occupy almost the same space. They have a smooth 1/f reduction, and are therefore suitable for reverse feedback of any strength. But this does not apply to the VMP 1! This is being operated here with a power loss amounting to 12W. The TO-3 housing has to be mounted on a cooling surface, with a mica disc as an intermediate layer, for heat extraction purposes. The resultant capacitance of approximately 150pF brings about a reduction of 2 degrees, so that the transistor will oscillate if the reverse feedback is too strong.

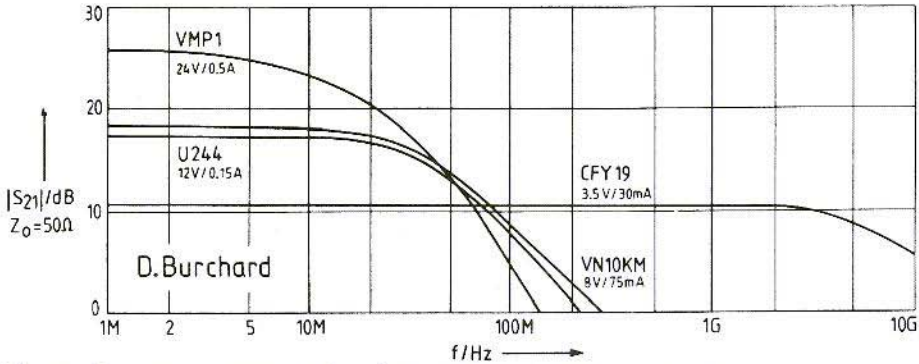

Fig.4: Scatter parameters S_{21} of some Field Effect Transistors

The S_{21} curves shown naturally have tolerances, but they are not defined further, even in the published lists. With the power FET's it is thoroughly established that the measured amplification is considerably smaller than that given in the data sheet. This is due to the fact that the steepness given there, measured using current pulses at 25° C., falls to under a half of the rated value if the crystal temperature rises by 100° K.

It can also be seen from the curves that the bipolar transistors are good for gain-blocks with an amplification of 20dB for a few tens of MHz's and for amplifications of 10dB for a few hundred MHz's. This is due to the fact that the transistors shown here have f_T at 5 GHz, whereas MMIC's contain transistors which are sometimes five times faster.

The power FET's provide gain-blocks which can be used above the limit of the high-frequency range (30 MHz).

4. CIRCUITS OF DIY GAIN-BLOCKS

A broad-band shortwave high-level stage as per (2) is also a gain-block, but one with a rather complicated internal

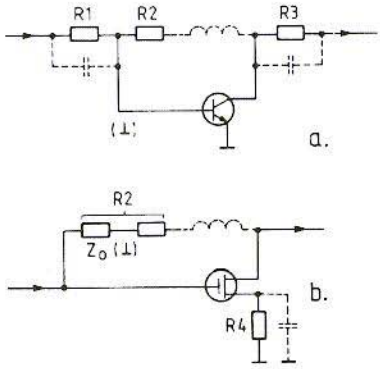

Fig.5: DIY Gain-Block circuit without components for setting the operating point. Components shown by dotted lines; improvement in upper frequency limit

a. with voltage feedback

b. with combined voltage and negative current feedback

circuit. If the idea is to create something which can compete with MMIC's, then only very simple circuits like those shown in Fig.5 come into question. Circuit 5a is particularly simple and the dimensions can be estimated. Circuit 5b gives better results in many cases. All components involved in the operating point setting have been omitted in the diagram, and we have also ignored the components shown by dotted lines to improve behaviour at high frequencies. Such improvements would not be possible with purchased gain-blocks.

Calculation bases for circuit 5a can be found, for example, in (3).

But things can be made even simpler! The transistor can be understood as being an inverting operational amplifier. A virtual zero point, ( ), forms at the base, due to the reciprocal coupling, R_2, and the output resistance becomes low. Preceding or succeeding resistances R_1 and R_3, with an order of magnitude of Z_o, match the system resistance. Now, the individual transistor is not as good an operational amplifier as you might wish. Its amplification reserve is rather small, its input resistance as per equation (2) is not high, and its output resistance is not low. The resistances, R_1 to R_3, must be corrected if we really want to obtain the desired amplification and the correct matching. The equations for this are given here, without any further explanation of how they are derived:

$$R_1 = Z_o - (1 - V)\frac{U_T}{I_c} \qquad (3)$$

$$R_2 = -2 \cdot V \cdot Z_o + (1 - V)\frac{U_T}{I_c} \qquad (4)$$

$$R_3 = Z_o - (1 - 2V)\frac{U_T}{I_c} \qquad (5)$$

Since the amplifier inverts, V should always be set negative. The first term after the equals sign is always the value for an internal amplification of any size, while the second is the corrective factor referred to above.

The calculation for the circuit as per Fig.5b can be found, for example, in (1). Here the transistor is operated with an emitter resistance, R_4, which lowers its steepness, S, to S_{red}.

$$S = I_c / U_T \qquad (6)$$

$$S_{red} = \frac{1}{R_4 + \frac{U_T}{I_c}} \qquad (7)$$

Many power transistors with multiple emitters already have built-in series resistances, which are primarily there to ensure that the current distribution is more uniform, but which also cause a reduction in steepness. They must be taken into consideration in this calculation. FET's, by their very nature, already have low steepness, and a reduction through R_4 is usually unnecessary. For every reduced steepness value, there is only one quite specific reciprocal coupling resistance, R_2, and thus also only one specific amplification, if the matching condition is to be fulfilled. The equations run as follows:

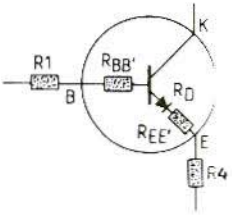

Fig.6: Noise sources in a Gain-Block

$$R_2 = S_{red} \cdot Z_o^2 = (1 - V)Z_o \qquad (8)$$

$$V = 1 - S_{red} \cdot Z_o = 1 - \frac{R_2}{Z_o} \qquad (9)$$

CFY 19 in Fig.4 has S = 33mS. Its amplification during matching is only -0.65. VN 10 KM has S = 75mS, and under the same conditions V = -2.75. Bipolar transistors have high steepness values, even when the collector current is low. If you wish to avoid having an external resistance, R_4, because then the emitter can be directly earthed, you must reduce the collector current until the desired degree of steepness is obtained. The condition required for this can be found by converting equation (6): $I_c = S \cdot UT$.

5. NOISE

In a DIY gain-block, noise comes not only from the semi-conductors but also from the resistances of the circuit, with one exception: resistance R_2 in Fig.5b does not contribute to the noise. This can be explained by the fact that a virtual zero point forms there. As pointed out in Fig.5, it can also be thought of as two individual resistances, Z_o and the remainder, put together. Both partial resistances make noise in a correlated way. The fraction from the left-hand partial resistance is amplified in the transistor and reversed in the phase, and then meets the noise fraction of the right-hand partial resistance at the collector, which brings about a nullification. The circuit is thus suitable for low-noise gain-blocks. Other noise sources are indicated in Fig.6. Apart from the resistances in the circuit, R_1 and R_4, these are the internal base feed resistance $R_{BB'}$ of the transistor, the internal emitter feed resistance $R_{EE'}$ and the differential conducting-state DC resistance of the BE-Diode R_D which is also the reciprocal value of the steepness:

$$R_D = \frac{1}{\quad} = \frac{U_T}{I_c} \qquad (10)$$

There is usually nothing in the data sheets about the sizes of $R_{BB'}$ and $R_{EE'}$. In GHz transistors, they are kept as small as possible, in order to improve the high-frequency behaviour. This leads to the curious result that many high-frequency transistors generate less noise in the low-frequency range than specially provided low-noise low-frequency transistors. On top of that, they are especially well suited to oscillator circuits, if low sideband noise values are required.

It can be demonstrated, from calculations and observations, that R_D makes half-thermal noise, and so its noise voltage is only as big as that of an ohmic resistance of half the value.

From all of that, we obtain, for the noise dimension of a gain-block with a bipolar transistor:

$$F/dB = 10\lg\left(1 + \frac{R_1 + R_{BB'} + 1/2R_D + R_{EE'} + R_4}{Z_o}\right) \quad (11)$$

A relationship as easy to monitor as this can not be laid down for amplifiers with FET's.

6. DISTORTION

When collector or drain currents are low, both bipolar and field effect transistors display an exponential transfer characteristic, i.e. a relationship between the output current and the input voltage, which can be expressed through an e-function. Bipolar transistors are often used in this range, but not usually FET's, and the former are no longer voltage-controlled when the collector current increases, because the input resistance falls.

From a limit which can be calculated using equation (2), with $R_{BE} = Z_o$, current source driving, which has a linearising effect, is increasingly present. At still higher current levels, ß is reduced and the characteristic curves in the opposite direction. Thus for many transistors there is an optimal collector current at which distortion values are low even without reciprocal coupling. This is the case, for example, for BFR 96 between 60 and 80mA.

The FET's used here work partly on a linear characteristic section (VMP1) or in a transitional area between this and the e-function area. U244 and VN 10 KM certainly have very attractive linear characteristics at higher current levels, but their limited lost heat extraction does not allow them to be continuously operated in these conditions.

It is very commonly said that distortion arising through reciprocal coupling can be traced back to a factor which corresponds to the amplification reserve. At low frequencies, this factor is naturally greater than the S_{21} curves of Figs. 3 and 4 show. The effect of this is that the values for the third-order intercept point (IM3) and for the 1dB compression point (P-1dB) are monotonically reduced at higher frequencies. This is just the same for purchased MMIC's, but is often not mentioned in data sheets.

If the active component is operating with a characteristic which can be described by an e-function, then there are specific natural relationships which it is worth remembering. We are not going to go through the derivation here, but rather give a short description of the approach. IM3 points and P-1dB points are connected to the third derivative of the characteristic. Using Taylor's method to develop the range, we obtain the coefficients of all mixed products during control using two frequencies. We can now preset the products which should appear at the output, and calculate the input voltage for them. Then, irrespective of the operating point selected on the e-function, we always get - 25dBm for the P_{-1dB} point,

i.e. an input voltage of 12.5mV. Whereas the IM3 point always turns out to be -7dBm, which means an input voltage of 100mV. Thus IM3 = P_{-1dB} + 18 dB is valid all the way through. For BFR 90/91/96 high-frequency transistors, all of which have a typical current amplification ß of 50, $R_{BE} = Z_o = 50\Omega$ when $I_c = 28mA$. If the collector current is lower than this, then without reverse feedback the gain-block will have the points calculated as characterising the distortion. With reverse feedback, they will lie higher, by the extent of the amplifier reserve.

The actual input power is not given only by the P_{-1dB} point at the input, but also by the modulation capability at the output. Not all the power generated goes into the load. A good part is destroyed in R2. The operating current and operating voltage must thus match one another and must be selected to be high enough for the output not to generate distortion at the input.

7. SOME PROVEN CIRCUITS

The isolating amplifier in Fig.7 is based on the circuit principle from Fig.5a. Good reverse damping is obtained by the virtual zero point at the base and the low output resistance at the collector. Since the amount of amplification is equal to 1, the output power to operate a pre-scaler can be low and the transistor also still operates very well at a collector voltage of 0.75V, the resulting circuit was simple. A few readings are also given.

The circuit as per Fig.8 certainly appears similar, but operates on the principle of Fig.5b. The collector current is selected in such a way that R4 can be dispensed with. It therefore does not contribute to the noise. The BFR 90 generates its minimum noise at a current level of 2mA. This circuit has the smallest noise dimension that can be obtained overall by this transistor in a 50Ω system. The only way to improve on it is to make the transition into a system with a Z_o which corresponds to the optimum generator resistance for this transistor.

Fig.9 shows a few more amplifiers. They all provide about 10dB amplification, but with widely varying output levels. At even higher power levels, chokes become necessary in the current supply, as is also required for many MMIC's, and more components are needed to set the operating point.

All the circuits illustrated will register a

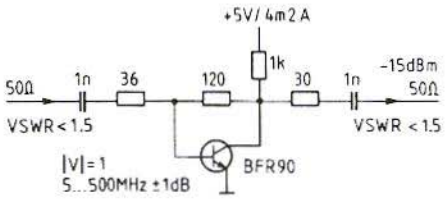

Fig.7: Isolating amplifier with V = 1 and particularly high isolation

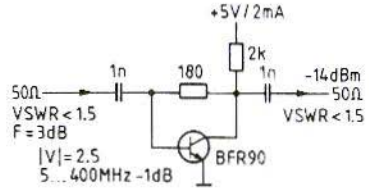

Fig.8: Low-noise small-signal amplifier with V = 2.5

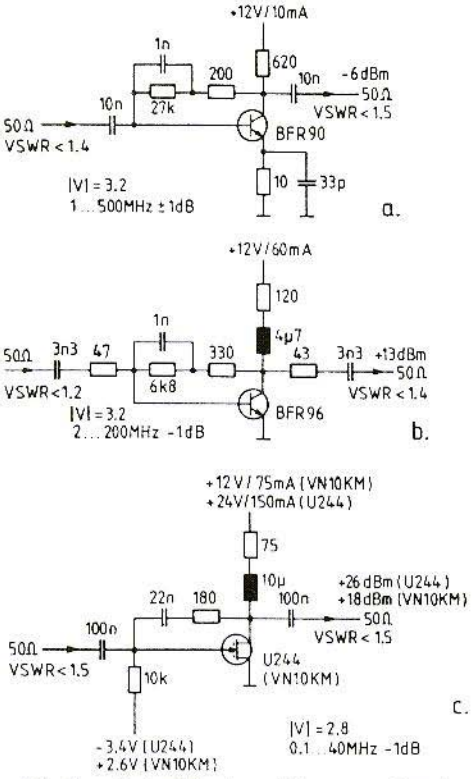

Fig.9: Gain-blocks with approximately 10dB amplification and greatly varying outputs:

a. with combined reverse feedback, bipolar

b. with voltage feedback, bipolar

c. with power FET's

more or less steep reduction in amplification as frequencies get higher. The reduction can be compensated for by one or more of the components shown by dotted lines in Fig.5 (then becoming all the steeper above). It is thus possible, with the transistors used here, to construct aerial amplifiers going right up to the top end of the television band V (800 MHz). But that is outside the scope of this article.

Dimensioning the compensation measures in Fig.5, which would generally not be possible with MMIC's, is best done empirically. At high frequencies, much is dependent on the location of the component. The inductance in series with R2 can simply consist of rather long connecting wires. The parallel capacitor at R4 is also dependent on whether the feed inductance to the emitter plays a role. In many applications it can be convenient to use transistors with two emitter connections. The capacitors lying parallel to R1 and R3 improve matching at high frequencies. Their value will lie between 10 and 33pF, if they are provided at all.

In principle, these amplifiers are stable with any reverse feedback. However, they often oscillate. Factors are involved which are not shown in the wiring diagram - increased switching capacity from base or collector to earth, resistances with excessive inductances (coiled formats) or excessive capacities to earth, and perhaps also too long an emitter supply line.